



Description

JMT N-channel Enhancement Mode Power MOSFET

Features

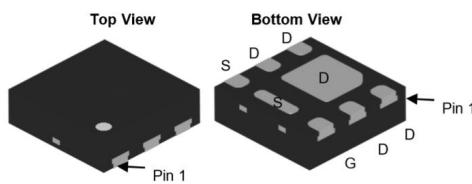
- 30V, 12A
- $R_{DS(ON)} < 12\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
- $R_{DS(ON)} < 18.5\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

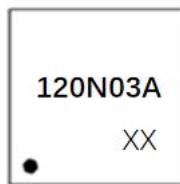
- Load Switch
- PWM Application
- Power management



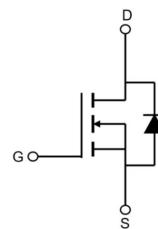
100% UIS TESTED!
100% ΔV_{ds} TESTED!



DFN2020-6L



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
120N03A	JMTV120N03A	TAPING	DFN2020-6L	7inch	3000	120000

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_c = 25^\circ\text{C}$	12	A
		$T_c = 100^\circ\text{C}$	7.8	A
I_{DM}	Pulsed Drain Current ^{note1}		48	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		20	mJ
P_D	Power Dissipation	$T_c = 25^\circ\text{C}$	9.6	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		13	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}$, $I_D=10\text{A}$	-	9.5	12	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=5\text{A}$	-	14.2	18.5	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	695	-	pF
C_{oss}	Output Capacitance		-	115	-	pF
C_{rss}	Reverse Transfer Capacitance		-	90	-	pF
Q_g	Total Gate Charge	$V_{DS}=15\text{V}$, $I_D=5\text{A}$, $V_{GS}=10\text{V}$	-	15	-	nC
Q_{gs}	Gate-Source Charge		-	2.5	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	3	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=15\text{V}$, $I_D=5\text{A}$, $R_{\text{GEN}}=3\Omega$, $V_{GS}=10\text{V}$	-	6.5	-	ns
t_r	Turn-on Rise Time		-	25	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	22	-	ns
t_f	Turn-off Fall Time		-	30	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	12	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	48	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s=12\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	8.5	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	2.6	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=15\text{V}$, $V_{GS}=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=9\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

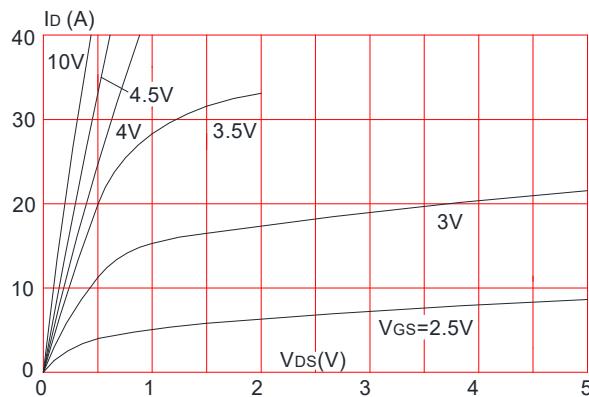


Figure 3: On-resistance vs. Drain Current

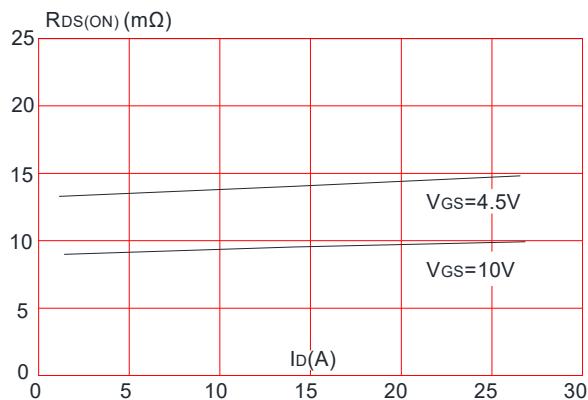


Figure 5: Gate Charge Characteristics

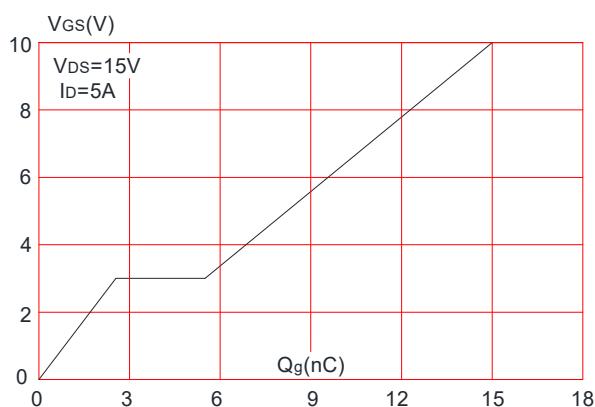


Figure 2: Typical Transfer Characteristics

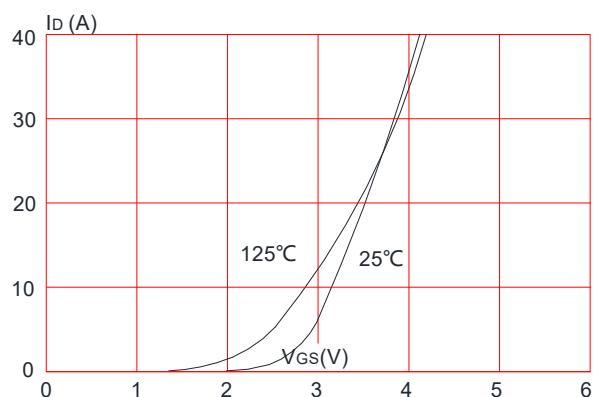


Figure 4: Body Diode Characteristics

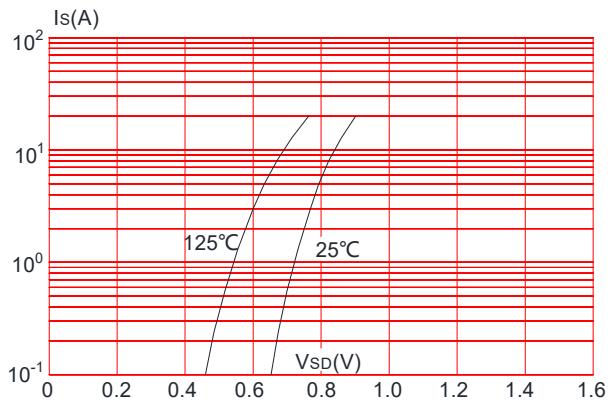


Figure 6: Capacitance Characteristics

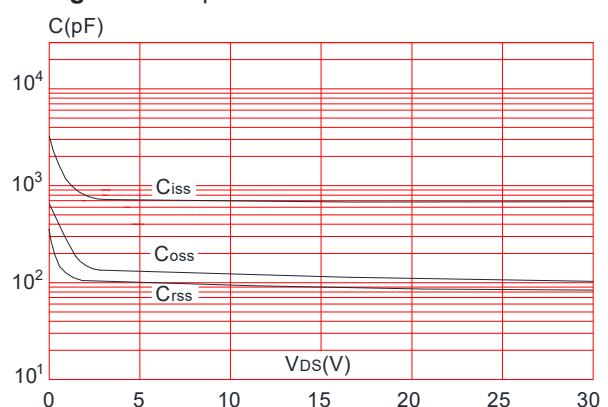


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

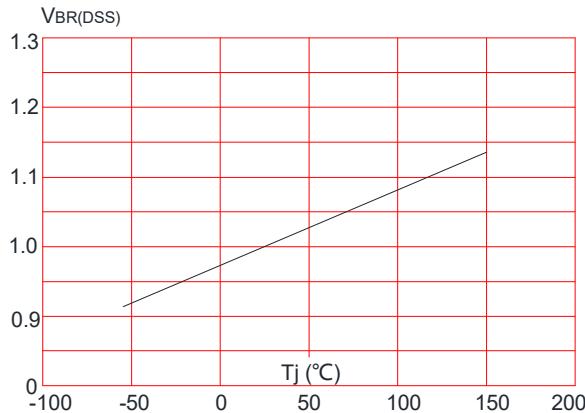


Figure 8: Normalized on Resistance vs. Junction Temperature

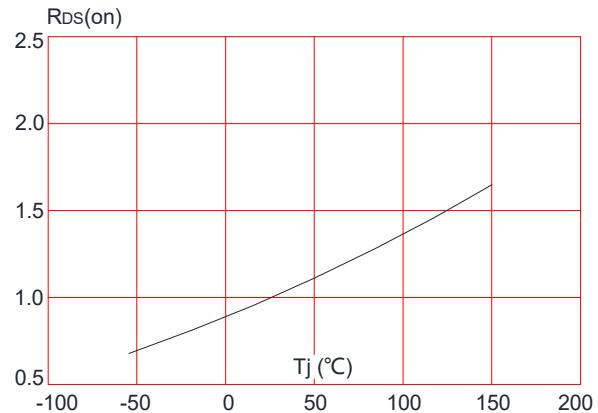


Figure 9: Maximum Safe Operating Area

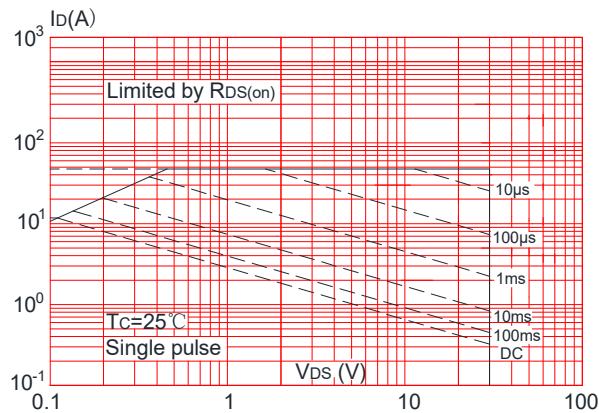


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

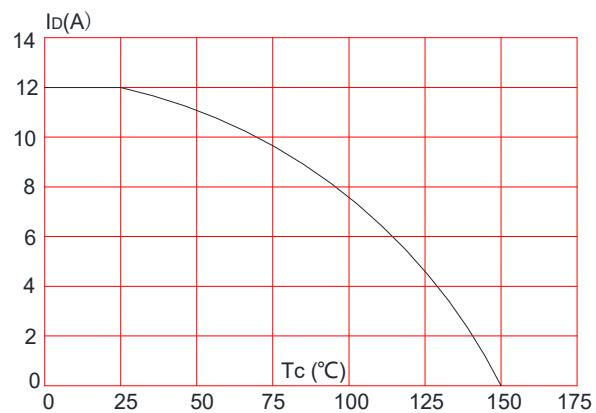
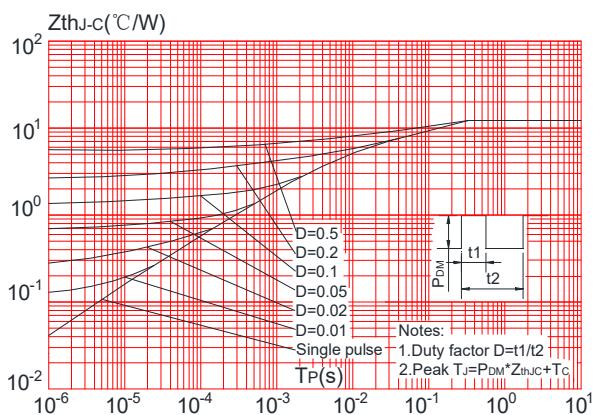


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

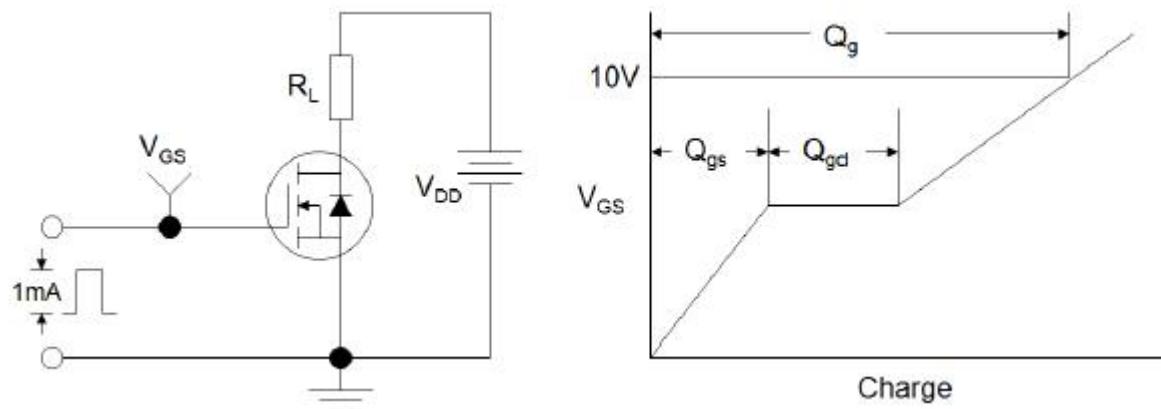


Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

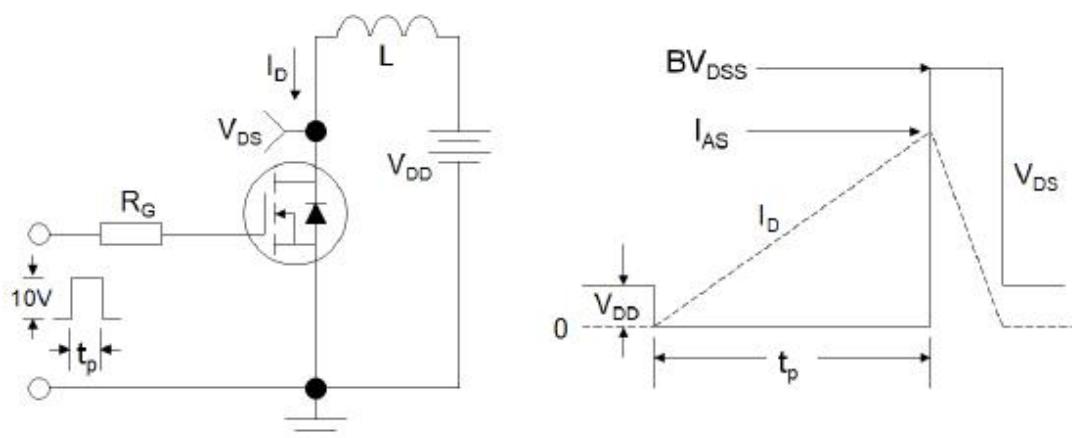
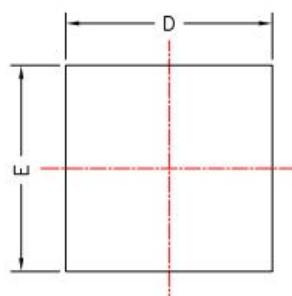


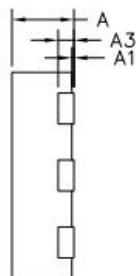
Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data- DFN2020-6L



Top View



Side View



Bottom View

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	---	---	0.002
A3	0.195	0.203	0.211	0.008	0.008	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65BSC			0.026 BSC		
D	1.900	2.000	2.100	0.075	0.079	0.083
E	1.900	2.000	2.100	0.075	0.079	0.083
D1	0.560	0.660	0.760	0.022	0.026	0.030
E1	0.250	0.350	0.450	0.010	0.014	0.018
D2	1.100	1.200	1.300	0.043	0.047	0.051
E2	0.900	1.000	1.100	0.035	0.039	0.043
L	0.150	0.250	0.350	0.006	0.010	0.014
L1	0.065	0.165	0.265	0.003	0.006	0.010
L2	0.000	0.100	0.200	0.000	0.004	0.008

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